## MTI #1737

## **CLAIMS:**

What is claimed is:

- 1 1. A method of operating a processor comprising the steps of:
- 2 mapping at least a portion of a program memory space to a data memory space;
- 3 storing an entry into the program memory space that is mapped to the data memory
- 4 space, the entry comprising data and a protection opcode;
- fetching an entry from the program memory space;
- 6 attempting to execute the fetched entry;
- 7 trapping the protection opcode;
- 8 vectoring to a trap handler; and
- 9 executing the trap handler.
- 1 2. The method of claim 1, wherein the trap handler is an illegal instruction trap
- 2 handler and the step of executing the trap handler comprises the steps of:
- determining that the opcode is a protection opcode; and
- 4 executing a software routine to handle the trap.
- 1 3. The method of claim 2, wherein the program memory space is internal to the
- 2 processor.
- 1 4. The method of claim 3, wherein the processor is operably connected to an external
- 2 memory device operable to store program instructions and data, the external memory
- 3 device comprising program memory space.

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- 1 5. The method of claim 1, wherein the trap handler is a protection trap handler.
- 1 6. The method of claim 5, wherein the program memory space is internal to the
- 2 processor.
- 1 7. The method of claim 6, wherein the processor is operably connected to an external
- 2 memory device operable to store program instructions and data, the external memory
- 3 device comprising program memory space.
- 1 8. A processor comprising circuitry operable to:
- 2 map at least a portion of a program memory space to a data memory space;
- 3 store an entry into the program memory space that is mapped to the data memory
- 4 space, the entry comprising data and a protection opcode;
- 5 fetch an entry from the program memory space;
- 6 attempt to execute the fetched entry;
- 7 trap the protection opcode;
- 8 vector to a trap handler; and

execute the trap handler.

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- 1 9. The processor of claim 8, wherein the trap handler is an illegal instruction trap
- 2 handler and the execution of the trap handler comprises:
- determining that the opcode is a protection opcode; and
- 4 executing a software routine to handle the trap.
- 1 10. The processor of claim 9, wherein the program memory space is internal to the
- 2 processor.
- 1 11. The processor of claim 10, wherein the processor is operably connected to an
- 2 external memory device operable to store program instructions and data, the external
- 3 memory device comprising program memory space.
- 1 12. The processor of claim 8, wherein the trap handler is a protection trap handler.
- 1 13. The processor of claim 12, wherein the program memory space is internal to the
- 2 processor.
- 1 14. The processor of claim 13, wherein the processor is operably connected to an
- 2 external memory device operable to store program instructions and data, the external
- 3 memory device comprising program memory space.